**NADIGOTTU RANJITH**

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**CARRER OBJECTIVE**

To secure a challenging role in a reputed organization that provides me with opportunities to apply and enhance my skills in digital design and verification. I aim to contribute to the development of high-quality and efficient digital designs by leveraging my academic knowledge, technical expertise, and passion for the field

**EDUCATION**

University College of Engineering Kakatiya University| Bachelor of technology YOP 2021

* Percentage :68%

Government Polytechnic College Kataram| Polytechnic Diploma YOP 2018

* Percentage :80%

Geervani High School| SSC YOP 2015

* Percentage :88%

**SKILLS**

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| HDL | : Verilog |
| HVL | : System Verilog |
| Software Tools | : Questasim |
| Operating System | : Linux |
| Programming Language | : C++ |

**KEY SKILLS**

Strong knowledge of digital electronics, computer architecture, Protocols (AXI, APB)

Good understanding of Verilog, System Verilog, UVM and can analyse and debug waveform.

**PROJECT**

**Project Title: Verification of Synchronous FIFO using System Verilog Testbench**

* System Verilog Testbench was designed to verify FIFO design with FIFO width of 8 bit and FIFO depth of 32.

My Role:

* Understanding the specification and features of FIFO
* Developed test plan for given FIFO design
* Developed various components of SV testbench and scenarios of FIFO features
* Simulation was done using Questasim Tool

**Project Title: Design, compilation and Simulation of a generic verification environment of an 8 Bit ALU**

* An 8-bit ALU was taken as DUT of this generic verification environment which was given random stimulus and the DUT along with the driver, generator, monitor and scoreboard class was compiled and simulated on Questasim.

My Role:

* Understanding the specification and features of ALU
* Developed test plan for given ALU design
* Developed various components of SV testbench and scenarios of ALU features
* Simulation was done using Questasim Tool

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| **Project Title** | **: VIP development of AMBA APB Protocol.** |

* APB is a part of the AMBA protocol family; it provides a low-cost interface that is optimized for minimal power consumption and reduces interface complexity. The APB interfaces to any peripherals that are low bandwidth and do not require the high performance of a pipelined bus interface.

My Role:

* Understanding the specification and features of APB protocol
* Developed test plan for both master and slave.
* Developed various components of SV testbench.
* Simulation is done using Questasim Tool.

**Project title: VIP development for AXI protocol using System Verilog**

* The AMBA AXI protocol is targeted at high-performance, High-frequency and includes a number of features such as separate address/control and data channels, burst based transactions with only start address issued. It supports out of order transactions, unaligned transfers and multiple outstanding addresses

My Role:

* Understanding the specifications and features of the AXI protocol
* Preparing the test plan
* VIP development for both slave and master in system Verilog
* Developed scenarios for various AXI features
* Developed BFM, monitor, generator, coverage.
* Developed cover groups and cover points for functional verification.
* Simulation & Debugging using Questasim Tool.

**Project title: Watchdog timer in Verilog**

* Description: Watchdog Timer checks if there is any hang situation in the design. If there is no activity timer keeps track of no activity time. If time of inactivity reaches a limit, it assumes that the system is truck, it generates a reset controller. So, the whole system will be reset. Also, it generates an interrupt to the processor. Without WDOG timer, there will be no one to keep track of system hang. It will continue to be in hang.

Roles and Responsibilities:

* Understanding the specifications and features of the WDOG timer
* Developed Verilog Test bench to verify WDOG timer
* Verified using various scenarios
* Simulation & debugging using Questasim Tool

**COURSE WORK**

* Digital Electronic, Analog Electronics, Signal & System, Cmos Vlsi Design, Computer Architecture

**ACHIEVMENTS AND RESPONSIBILITES**

* Served as a volunteer for Social Service of Blind people Organisation.
* Secured 2nd position in Inter college Chess tournament.

**DECLARATION**

* I hereby declare that the above information is correct to the best of my knowledge and that I will be held responsible for any deviation from them at a later stage.

**Nadigottu Ranjith**